Listing of the Claims:

Claim 1 (Original): A semiconductor memory device comprising:

a first insulating layer having a gate electrode on a semiconductor substrate;

a second insulating layer formed on the first insulating layer, the second insulating layer having bit lines covered with bit line isolation layers, buried contact plugs formed between the bit lines, and a first metal contact plug connected to the semiconductor substrate through the first insulating layer;

a silicon nitride layer on the second insulating layer; and

a third insulating layer formed on the silicon nitride layer, the third insulating layer having a second metal contact plug connected to the first metal contact plug through the silicon nitride layer.

Claim 2 (Original): The device of claim 1, wherein the second insulating layer further comprises a first landing stud connected to the gate electrode through the first insulting layer.

Claim 3 (Original): The device of claim 2, wherein the bit lines comprise a direct contact plug under one of the bit line.

Claim 4 (Original): The device of claim 3, wherein the first landing stud is simultaneously formed with the direct contact plug.

Claim 5 (Original): The device of claim 2, wherein the second insulating layer further comprises a second landing stud on the first landing stud.

Claim 6 (Original): The device of claim 5, wherein the second landing stud is larger in surface area than the first landing stud.

Claim 7 (Original): The device of claim 1, wherein the first metal contact plug and the buried contact plugs are simultaneously formed with an electrical conducting material.

Claim 8 (Original): The device of claim 7, wherein the electrical conducting material includes tungsten (W).

Claim 9 (Original): The device of claim 1, wherein the third insulating layer further comprises a metal-insulator-metal capacitor on the buried contact plug.

Claims 10-23 (Canceled)